WHAT IS CLAIMED IS:

1. A power supply multiplexing circuit comprising:

a first supply voltage input;

a first pair of cascoded PMOS transistors in series with the first supply voltage input;

a first native NMOS transistor in series with the first pair of cascoded PMOS transistors;

a second supply voltage input;

a second pair of cascoded PMOS transistors in series with the second supply voltage input; and

a second native NMOS transistor in series with the second pair of cascoded PMOS transistors,

wherein the gates of the first and second native NMOS transistors are driven by two control signals out of phase with each other, and

wherein sources of the first and second native NMOS transistors are connected together to output an output voltage.

2. The power supply multiplexing circuit of claim **1**, wherein gates of the first pair of the cascoded PMOS transistors are connected together and to a gate of the second native NMOS transistor.

3. The power supply multiplexing circuit of claim **2**, wherein gates of the second pair of the cascoded PMOS transistors are connected together and to a gate of the first native NMOS transistor.

4. A power supply multiplexing circuit comprising:

two half-cells, each half cell including:

a first supply voltage input;

in series, a first cascoded PMOS transistor connected to a corresponding supply voltage,

a second cascoded PMOS transistor, and

a native NMOS transistor;

wherein the gates of the native NMOS transistors are driven by two control signals out of phase with each other, and

wherein sources of the first and second native NMOS transistors are connected together to output an output voltage.

5. The power supply multiplexing circuit of claim **4**, wherein gates of each of the first and second cascoded PMOS transistors are connected together and to a gate of the native NMOS transistor.

6. A power supply multiplexing circuit comprising:

a first pair of PMOS transistors in series with a first voltage input;

a first native NMOS transistor in series with the first pair of PMOS transistors;

a second pair of PMOS transistors in series with a second voltage input; and

a second native NMOS transistor in series with the second pair of PMOS transistors,

wherein the gates of the first and second native NMOS transistors are driven by two control signals out of phase with each other, and

wherein sources of the first and second native NMOS transistors are connected together.

7. The power supply multiplexing circuit of claim **6**, wherein gates of the first pair of the PMOS transistors are connected together and to a gate of the second native NMOS transistor.

8. The power supply multiplexing circuit of claim **7**, wherein gates of the second pair of the PMOS transistors are connected together and to a gate of the first native NMOS transistor.